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10/085,646

Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers | Preferences | Cases

Search Results -

Terms	Documents
L2 and (gate adj electrode) and source and drain and (gate adj dielectric) and sidewalls	5

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L3

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Search History

DATE: Sunday, September 08, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=OR		
L3	L2 and (gate adj electrode) and source and drain and (gate adj dielectric) and sidewalls	5	L3
L2	L1 and (oxide near2 layers) and (nitride near2 layers)	124	L2
L1	(self adj aligned) near2 (interconnects or interconnections)	233	L1

END OF SEARCH HISTORY

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Search Results - Record(s) 1 through 5 of 5 returned.

☐ 1. Document ID: US 6376344 B1

L3: Entry 1 of 5 File: USPT Apr 23, 2002

US-PAT-NO: 6376344
DOCUMENT-IDENTIFIER: US 6376344 B1

TITLE: Semiconductor device with fully self-aligned local interconnects, and method for fabricating the device

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 2. Document ID: US 6287951 B1

L3: Entry 2 of 5 File: USPT Sep 11, 2001

US-PAT-NO: 6287951
DOCUMENT-IDENTIFIER: US 6287951 B1

TITLE: Process for forming a combination hardmask and antireflective layer

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 3. Document ID: US 5792687 A

L3: Entry 3 of 5 File: USPT Aug 11, 1998

US-PAT-NO: 5792687
DOCUMENT-IDENTIFIER: US 5792687 A

TITLE: Method for fabricating high density integrated circuits using oxide and polysilicon spacers

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

☐ 4. Document ID: US 5589412 A

L3: Entry 4 of 5 File: USPT Dec 31, 1996

US-PAT-NO: 5589412
DOCUMENT-IDENTIFIER: US 5589412 A

TITLE: Method of making increased-density flash EPROM that utilizes a series of planarized, self-aligned, intermediate strips of conductive material to contact the drain regions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

☐ 5. Document ID: US 5360757 A

L3: Entry 5 of 5 File: USPT Nov 1, 1994

US-PAT-NO: 5360757
DOCUMENT-IDENTIFIER: US 5360757 A

TITLE: Process for fabricating a self aligned interconnect structure in a semiconductor device

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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Terms	Documents
L2 and (gate adj electrode) and source and drain and (gate adj dielectric) and sidewalls	5

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